BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Institute affiliated to VTU, Belagavi, Approved by AICTE, New Delhi)

Avalahalli, Yelahanka, Bengaluru 560064

Bachelor of Engineering

Department of Electronics and Communication Engineering

V and VI Semester Scheme and Syllabus
2021 Scheme - Autonomous

Approved in the BoS meeting held on 22.05.2023

Vision and Mission of the Department

Vision

Be a pioneer in providing quality education in electronics, communication, and allied engineering fields to serve as a valuable resource for industry and society

Mission

1. Impart sound theoretical concepts and practical skills through innovative pedagogy

2. Promote Interdisciplinary Research

3. Inculcate Professional Ethics

Program Educational Objectives (PEOs)

1. Work as Professionals in the area of Electronics, Communication and Allied Engineering Fields.
2. Pursue Higher Studies and involve in Interdisciplinary Research Work.
3. Exhibit Ethics, Professional Skills and Leadership Qualities in their Profession.

Program Specific Outcomes (PSOs)

1. Demonstrate the knowledge of electronic devices, circuits, micro-nano electronics and other fundamental courses to exhibit competency in the domain of VLSI design.
2. Comprehend the gathered knowledge and technological advancements in the field of communication and signal processing.
3. Exhibit the skills gathered to analyze, design, develop software applications and hardware products in the field of embedded systems and allied areas.

BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

(An Autonomous Institution affiliated to VTU, Belagavi)
Yelahanka, Bengaluru-560064

Date: 14.06.2023

CIE and SEE Pattern for 2021 Scheme
(Applicable from the AY 2021-22 onwards)

Important Note:

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Examinations (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for SEE minimum passing mark is 35% of the maximum marks (18 marks out of 50). The student is declared as a pass in the course if he / she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

4 CREDIT and 3 CREDIT COURSES

I. CONTINUOUS INTERNAL EVALUATION (CIE): 50 MARKS

- Internal Assessment (IA) Tests: 3 IAs to be conducted for 40 Marks (90 minutes each). Total of 3 tests will be 120 and the same can be scale down to **60 marks.**
- Alternate Assignment Tool (AAT): 2 AATs each of 10 marks, total **20 marks.**
- Assignments: 2 assignments of each 10 marks, total **20 marks**.
- CIE marks = 60 + 20 + 20 = 100 and same can be scale down to **50 marks.**
- Student has to score minimum of 20 marks (40%).

II. SEMESTER END EXAMINATIONS (SEE): 50 MARKS

SEE is conducted for 100 Marks (3 hours).

Question Paper Pattern:

Part - A: Comprises 20 objective type questions carrying 1 Mark each with a total 20 Marks.

Part - B: There will be **5 modules**. Each module will have **TWO questions carrying 16 marks** each. There will be a maximum of three sub section for each question. **Student has to answer any ONE full question from each module.**

SEE Marks = 20 + 80 = 100 marks and can be scale down to 50 marks.

2 CREDIT COURSES

I. CONTINUOUS INTERNAL EVALUATION (CIE): 50 MARKS

- Internal Assessment (IA) Tests: 3 IAs of MCQ type to be conducted for 40 Marks (60 minutes each). Total of 3 tests will be 120 and the same can be scale down to **60 marks.**
- Alternate Assignment Tool (AAT): 2 AATs each of 10 marks, total **20 marks**.
- Assignments: 2 assignments of each 10marks, total **20 marks.**
- CIE marks = 60 + 20 + 20 = 100 and same can be scale down to **50 marks.**
- Student has to score minimum of 20 marks (40%).

II. SEMESTER END EXAMINATIONS (SEE): 50 MARKS

SEE is conducted for 100 Marks (2 hours).

Question Paper Pattern:

- The pattern of the question paper is MCQ.
- SEE question paper will be set for 100 questions each of 01 marks. The same is scale down to 50 marks.

1 CREDIT COURSES

I. CONTINUOUS INTERNAL EVALUATION (CIE): 50 MARKS

- Internal Assessment (IA) Tests: 3 IAs of MCQ type to be conducted for 40 Marks (60 minutes each). Total of 3 tests will be 120 and the same can be scale down to **60 marks.**
- Alternate Assignment Tool (AAT): 2 AATs each of 10 marks, total **20 marks.**
- Assignments: 2 assignments of each 10marks, total **20 marks.**
- CIE marks = 60 + 20 + 20 = 100 and same can be scale down to **50 marks.**
- Student has to score minimum of 20 marks (40%).

II. SEMESTER END EXAMINATIONS (SEE): 50 MARKS

SEE is conducted for 50 Marks (1 hours).

Question Paper Pattern:

- The pattern of the question paper is MCQ.
- SEE question paper will be set for 50 questions each of 01marks. The same is scale down to 50 marks.

1 CREDIT LABORATORY COURSES

I. CONTINUOUS INTERNAL EVALUATION (CIE): 50 MARKS

- Cumulative Assessment (CA) of each experiment is 20 Marks (Conduction 10 marks + Records 5 marks +Viva 5marks). The average of all the experiments to be taken for **20 marks.**
- Open Ended Experiments (OE) **10 marks.**
- 2 IAs Test to be conducted for 100 marks. General rubrics suggested for SEE are: Writeup 20 marks, Conduction of the experiments, calculations, graphs, results, etc.,: 60 marks and Viva: 20 marks. The average of 2 IA marks is scale down to **20 marks**.
- CIE marks =20 (CA) +10 (OE) + 20 (IA test) = 50 marks.
- Student has to score minimum of 20 marks (40%).

II. SEMESTER END EXAMINATIONS (SEE): 50 MARKS

SEE is conducted for 100 Marks and scale down to 50 Marks.

Examinations to be conducted jointly by Two examiners. All the experiments are to be included for practical examination. General rubrics suggested for SEE are: Writeup 20 marks, Conduction of the experiments, calculations, graphs, results, etc.,: 60 marks and Viva: 20 marks.

CoE 16/06/2023 Dean AA 16/06/2023 Principal 19/6/23

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Institute affiliated to VTU)

Scheme of Teaching and Examination: Effective from AY 2021 – 22

Choice Based Credit System (CBCS)

UG PROGRAM: ELECTRONICS AND COMMUNICATION ENGINEERING (ECE) — **Semester: VI**

Sl. No	Course Category	Course Code	Course Title	Teaching Dept.	Teaching Hours /Week				Credits	Examination			
					L	T	P	PW		Duration	CIE Marks	SEE Marks	Total Marks
1	HS	21HSS61	Project and Finance Management	ECE	2	0	0	0	2	2	50	50	100
2	AEC	21AEC62	Bioinformatics	ECE	1	0	0	0	1	1	50	50	100
3	AEC	21EC63	Green Technologies	ECE	0	2	0	0	1	1	50	50	100
4	PE	21EC64X	Professional Elective – II	ECE	3	0	0	0	3	3	50	50	100
5	OE	21EC65X	Open Elective - I	ECE	3	0	0	0	3	3	50	50	100
6	PW	21EC66	Mini Project	ECE	0	0	0	4	2	3	50	50	100
7	PC	21EC67	Advanced Communication Theory	ECE	2	2	0	0	3	3	50	50	100
8	PC	21EC68	VLSI Design	ECE	4	0	0	0	4	3	50	50	100
9	PC	21ECL69A	Advanced Communication Laboratory	ECE	0	0	2	0	1	3	50	50	100
10	PC	21ECL69B	VLSI Laboratory	ECE	0	0	2	0	1	3	50	50	100
TOTAL					**15**	**4**	**4**	**4**	**21**		**500**	**500**	**1000**

Professional Elective - Group II	
Course Code	**Course Title**
21EC641	Computer Communication Networks
21EC642	Mathematics for Machine Learning-II
21EC643	Embedded System Design
21EC644	Artificial Neural Networks
21EC645	Mobile Communication
21EC646	VLSI Verification

Open Elective (OE) - Group I	
Course Code	**Course Title**
21EC651	Cellular Mobile Communication
21EC652	Sensors and Applications
21EC653	Signal Processing and Applications
21EC654	Embedded Controllers and Applications
21EC655	8051 Microcontroller
21EC656	Industrial Electronics

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Syllabus

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER - VI

Project and Finance Management (2:0:0) 2

(Effective from the academic year 2020-21)

Course Code	**21HSS61**	CIE Marks	50
Teaching Hours/Week (L:T:P)	2:0:0	SEE Marks	50
Total Number of Contact Hours	25	Exam Hours	02

Course Objectives:

This course will enable students to:

1. Define the fundamentals of Project Management.
2. Identify the strategies involved in selection, prioritization, planning & scheduling of a project.
3. Understand the time value of money & apply it for decision making.
4. Analyse project risk, progress & results.
5. Make awareness about various sources of finance.
6. Gain Knowledge on working capital & capital budgeting.

Module – 1

Preamble: Project Management: Need for project management, management practices to meet the challenges of new economic environment, globalization process, rapid technological advancement, and quality concerns of the stakeholders.

Project Management: Definition of project, characteristics of projects, types of projects, project roles.

Project Selection & Prioritization: Strategic planning process, strategic objectives, identifying potential projects, feasibility study (environment, society), methods of selecting projects, prioritizing projects, securing and negotiating projects.

(05 Hours)

Module – 2

Project planning & scheduling: Project scope & check list, work break down structure, project schedule, uncertainty in project schedules.

Project resourcing & risk planning: Abilities needed when resourcing projects, estimate resource needs, cost planning & estimating, risk management planning, risk identification, risk analysis, project quality planning and project kick-off.

(05 Hours)

Module – 3

Project performing, progress & results: Project supply chain management, project balanced score card approach, terminate project early, finish project, customer feedback & approval.

(05 Hours)

Module – 4

Financial Management: Evolution of financial management, key activities of finance manager, key decision areas in financial management, financial statement with balance sheet. Efficient utilization and generation of monetary resources and funds, a comparative study of finance and economics, Costs and revenue evaluation for various engineering operations.

Capital Budgeting: Types of capital budgeting decisions, capital budgeting proposals, estimating cash flows for project appraisal, green capital budgeting.

(05 Hours)

Module – 5

Working capital management: Factors affecting working capital requirement, operating cycle analysis, negative working capital, cash planning & managing cash flows.

Cost of capital and leverage Analysis: Concept, significance, assumptions, factors affecting cost of capital, Leverage Analysis: operating leverage, financial leverage.

Recap: All the 5 modules. (05 Hours)

Course outcomes:

The students will be able to:

CO1: Understand the selection, prioritization & initiation of individual projects.
CO2: Understand WBS, scheduling, uncertainty & risks associated in project.
CO3: Identify & Evaluate the progress and results of the project.
CO4: Understand time value of money & use it for decision making.
CO5: Outline capital requirements for starting a business & management of working capital.

Textbooks

1. Timothy J Kloppenborg, Project Management, Cengage Learning, 2nd Edition, 2009.

2. John J Hampton, Financial Management, PHI Publication, 4th edition.

References

1.Pennington Lawrence, Project Management, McGraw-Hill, 1st edition.

2.Joseph A Moder, Philips New Yark, Project Management with CPM & PRT, McGraw-Hill, 2nd edition, 1983.

3.Harold Kerzner, Project Management A system approach to Planning, Scheduling & Controlling, CBS Publication, 2nd Edition,2006.

4.S.D. Sharma, Operations Research, Kedar Nath Ramnath, Meerut, New Edition,2015.

5.M.Y. Khan, Financial Management, Tata Mc-Graw Hill, Fifth Edition,2007.

6. O.P. Khanna, Industrial Engineering & Management, Dhanpat Rai Publications, Second Edition, 1999.

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER VI

Bioinformatics (1:0:0) 1

(Effective from the academic year 2023-24)

Course Code	**21AEC62**	CIE Marks	50
Teaching Hours/Week (L:T:P)	1:0:0	SEE Marks	50
Total Number of Contact Hours	15	Exam. Hours	1

Course Objectives:

1. Better understanding of dynamic biological processes and their understanding at molecular level enabled through and correlated using internet and Bioinformatics.
2. To relate the basic knowledge in Genetics & Molecular Biology and see how it can be applied through Bioinformatics perspective.
3. To utilize bioinformatics tools and databases for retrieving, analyzing, understanding and managing biological data.

Module – 1

Preamble: Bioinformatics is an interdisciplinary field mainly involving molecular biology and genetics, computer science, mathematics, and statistics. Data intensive, large-scale biological problems are addressed from a computational point of view.

Biological Data Acquisition

The form of biological information. Retrieval methods for DNA sequence, protein sequence and protein structure information

(3 Hours)

Module – 2

DATABASES

Format and Annotation: Conventions for database indexing and specification of search terms, Common sequence file formats. Annotated sequence databases – primary sequence databases, protein sequence and structure databases, Organism specific databases.

(3 Hours)

Module – 3

DATA PROCESSING

Data – Access, Retrieval and Submission: Standard search engines; Data retrieval tools – Entrez, DBGET and SRS; Submission of (new and revised) data; Sequence Similarity Searches: Local versus global. Distance metrics. Similarity and homology. Scoring matrices.

(3 Hours)

Module – 4

METHODS OF ANALYSIS

Dynamic programming algorithms, Needleman-wunsch and Smith-waterman. Heuristic Methods of sequence alignment, FASTA, and PSI BLAST.

(3 Hours)

Module – 5

APPLICATIONS

Genome Annotation and Gene Prediction; ORF finding; Phylogenetic Analysis: Comparative genomics, orthologs, paralogs.

(3 Hours)

Course Outcomes:

The students will be able to:

1: Apply the basic methodology in Bioinformatics to retrieve data.
2: Analyse bioinformatics tools and databases for understanding and managing biological data.
3: Examine the applications of bioinformatics in allied areas.

Textbooks:

1. Introduction to Bioinformatics by Arthur K. Lesk , Oxford University Press.
2. Algorithms on Strings, Trees and Sequences by Dan Gusfield, Cambridge University Press.
3. Biological Sequence Analysis Probabilistic Models of proteins and nucleic acids by Durbin, S.Eddy, A.Krogh, G.Mitchison.
4. Bioinformatics Sequence and Genome Analysis by David W. Mount, Cold Spring Harbor Laboratory Press.
5. Beginning Perl for Bioinformatics: An introduction to Perl for Biologists by James Tindall, O"Reilley Media.

References:

1. Bioinformatics The Machine Learning Approach by Pierre Baldi and Soren Brunak.

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER - VI

Green Technologies (0:2:0) 1

(Effective from the academic year 2021-22)

Course Code	**21EC63**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:2:0	SEE Marks	50
Total Number of Contact Hours	15	Exam Hours	01

Course Objectives:

This course will enable students to:

1. Analyze energy efficient communication systems such as Telecommunication systems, ICT, Wireless networks and cellular networks by understanding the principles of green communications.
2. Understand the impact of conventional energy sources on the environment and realize the significance and principles of green energy sources for sustainability.

Module – 1

Green Communications: Introduction, Origin of Green Communications, Energy Efficiency in Telecommunication systems: Telecommunication system model and energy Efficiency, Energy saving concepts.

GREEN ENERGY: Introduction, green energy systems - composition, adverse impacts, Green energy and sustainability, the target and solution. Energy sources and their availability, Green energy sources - solar energy, wind energy, geothermal energy, ocean energy, biomass and biogas. (07 Hours)

Module – 2

Green Building: Concept, Necessity, Characteristics, Benefits, Requisites for green building construction, Sustainability, Concept of REDUCE, REUSE, RECYCLE, RETHINK, REPLENISH AND REFUSE (6 R's),

GREEN MANUFACTURING: Green Manufacturing - Introduction, Background and Definition. Impact of traditional manufacturing in environmental ecology, Need for green manufacturing, Advantages and Limitations of green manufacturing.

Concept, History, scientific approach, elements of vastu for selecting a plot. Indian Green Building Council. (08 Hours)

Course Outcomes:

CO1: Realise the importance of green technologies in sustainable growth of Industry and society

CO2: Design and implementation of suitable energy efficient processes.

CO3: Plan and use of selective materials for green buildings.

Textbooks

1. Konstantinos Samdanis, Peter Rost, Andreas Maeder, MichelaMeo, Christos Verikoukis, Green Communications: Principles, Concepts and Practice, John Wiley & Sons, 2015.
2. J Paulo Davim, Green Manufacturing: Processes and Systems, Springer, 2012.

Reference Books

1. G.D. Rai, Non-conventional Energy Sources, Khanna Publishers, Delhi, 5th Edition, 2011.
2. San Murugesan, G.R. Gangadharan, Harnessing Green IT – Principles and Practices, John Wiley & Sons Ltd., 2008.
3. Tom Woolley, Sam Kimmins, Paul Harrison and Rob Harrison, Green Building Handbook, Volume 1, E & FN Spon, an imprint of Thomson Science & Professional.
4. David A Dornfeld, Green Manufacturing: Fundamentals and Applications, Springer, 2013.

COs and POs Mapping

CO	PO											
	1	2	3	4	5	6	7	8	9	10	11	12

CO1		2										
CO2			3									
CO3				3								2

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Computer Communication Networks (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC641**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course Objectives:

This course will enable students to

1. Understand the layering architecture of OSI reference model and TCP/IP protocol suite with associated protocols.
2. Familiarize with the header formats, routing protocols and transport layer services.
3. Analyse various protocols, algorithms for different networking architectures.
4. Design a network for various network parameters using simulation tools.

Module – 1

Significance and scope of Computer Communication Networks in current scenario, industry applications, research and innovations related to the course and impact of course on societal problems.

Introduction to computer networking:

Data Communications: Components, Representations, Data Flow, Networks: Physical Structures, Network Types: LAN, WAN.

Network Models: Protocol Layering: TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and De-multiplexing, The OSI Model: OSI Versus TCP/IP.

Data-Link Layer: Introduction, Link Layer addressing: Types of addresses, Data Link Control (DLC) services: Framing, Flow and Error Control, Simple Protocol, Stop and Wait protocol, go back N protocol, selective repeat protocol.

Tools: Use Wireshark tool as network analyzer. (8 Hours)

Module – 2

Media Access Control:

Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Wired LANs: Ethernet: Ethernet Protocol: IEEE802, Ethernet Evolution, Standard Ethernet: Characteristics, Addressing, Access Method, Efficiency, Implementation,

Connecting Devices:

Hubs, Switches, Routers. Virtual LANs: Membership, Configuration, Communication between Switches and Routers, Advantages. (8 Hours)

Module – 3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

Network Layer Protocols:

Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security ofIPv4 /6 Datagrams Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. Virtual Private Network, Security in VPN.

(8 Hours)

Module – 4

Transport Layer: Introduction, Transport Layer Services, Connectionless and Connection oriented Protocols, User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control, Techniques to improve QOS.

(8 Hours)

Module – 5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client – Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging. Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS

(8 Hours)

Summary of the Course: The student will be able to understand the concepts of computer network, network models, protocols and algorithms.

Course Outcomes: The students will be able to:

CO1: Understand the concepts of computer networks like network models, addresses, channels, nodes and topologies.

CO2: Apply the knowledge of communication channels, protocols, algorithms for data communication.

CO3: Analyse the characteristics of communication channels, protocols, algorithms for data communication.

CO4: Interpret the given case study material for network structure and protocols.

CO5: Perform in a **group** to **design** a data communication network using network simulator.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Data Communications and Networking 5th Edition	B.Forouzan	McGraw Hill	2020	**Text**
Computer Networks	James J Kurose, Keith W Ross	3rd Edition, Pearson Education	2013	**Reference**
Introduction to Data Communication and Networking	Wayarles Tomasi	3rd Edition, Pearson Education	2007	**Reference**

COsandPOsMapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	1											
CO2	2											
CO3	2	1										
CO4	2	1		1								
CO5	3	3	2		3			2	2	2		2

Level3- HighlyMapped, Level 2-ModeratelyMapped, Level1-LowMapped, Level0-NotMapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Mathematics for Machine Learning – II (3:0:0) 3
(Effective from the academic year 2021-22)

Course Code	**21EC642**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course objectives:

This course will enable students to:

1. Understand probability and random variables, including discrete and continuous probabilities.
2. Apply optimization techniques, such as gradient descent, momentum, stochastic gradient descent, convex optimization, linear programming, and quadratic programming.
3. Develop a strong foundation in data, models, and learning.
4. Master linear regression techniques, including problem formulation, parameter estimation, handling overfitting etc.
5. Gain proficiency in dimensionality reduction techniques.

Module – 1

Probability and distributions: Probability and Random Variables, Discrete and Continuous Probabilities, Sum Rule, Product Rule, and Bayes' Theorem, Means and Covariances, Empirical Means and Covariances, Sums and Transformations of Random Variables, Inner Products of Random Variables.

Module – 2

Continuous Optimization: Optimization Using Gradient Descent, Step-size, Gradient Descent With Momentum, Stochastic Gradient Descent, Convex Optimization, Linear Programming, Quadratic Programming.

Module – 3

Data, Models, and Learning: Data as Vectors, Models as Functions, Models as Probability Distributions, Empirical Risk Minimization, Hypothesis Class of Functions, Loss Function for Training, Regularization to Reduce Overfitting, Cross-Validation to Assess the Generalization Performance,

Module – 4

Linear Regression: Problem Formulation, Parameter Estimation, Maximum Likelihood Estimation, Overfitting in Linear Regression, Bayesian Linear Regression

Module – 5

Dimensionality Reduction: Principal component analysis: problem setting, Maximum Variance Perspective, Projection Perspective, Eigenvector Computation and Low-Rank Approximations, PCA in High Dimensions, Key Steps of PCA in Practice

Course Outcomes: The students will be able to:

CO1:	Understand foundational concepts of probability and random variables, optimization techniques, data representation, linear regression, and principal component analysis.
CO2:	Apply the knowledge of linear algebra, probability, optimization in generating the data and models used in machine learning
CO3:	Analyze and solve problems related to probability, optimization, data analysis, linear regression, and dimensionality reduction.
CO4:	Interpret the given case study situation related to applications of mathematics in machine learning

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Mathematics for Machine Learning	Marc Peter Deisenroth , A. Aldo Faisal , Cheng Soon Ong	Cambridge University Press	**2020**	Text
Linear Algebra and Optimization for Machine Learning	Charu C. Aggarwal	Springer	2020	Reference

COs and POs Mapping

CO	PO														
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2												3	
CO2	2	3		2										3	
CO3	3	3		2										3	
CO4	3	2		2						2		3		3	

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Embedded System Design (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC643**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course objectives:

This course will enable students to:

1. Understand the basics of memory, I/O systems and Architecture.
2. Learn the different system models and processors.
3. Study the functionality of multitasking
4. Design embedded applications.

Module – 1

Introduction: To Embedded System, significance and scope of Embedded System, in current scenario, industry applications, research and innovations related to Embedded System and impact of course on societal problems.

A System Engineering Approach to Embedded Systems Design:

Introduction to Embedded Systems Architecture, The Embedded Systems Models, Embedded Hardware building blocks, Reading a Schematic.

(9 Hours)

Module – 2

Embedded Processors & Memory:

ISA Architecture Models: Application specific, Internal Processor Design, Processor Performance, Reading Processors, Datasheet, ROM, RAM, Cache Memory, Cache mapping techniques, Memory Management of External Memory, Board Memory and Performance

(7 Hours)

Module – 3

Board I/O & Buses:

Managing Data: Serial vs. Parallel I/O, Interfacing the I/O Components, I/O and Performance, Bus Arbitration and Timing, I2C, SPI, USB, CAN & PCI protocols, integrating the Bus with Other Board Components, Bus Performance.

(7 Hours)

Module – 4

Embedded Software and RTOS

Device Drivers: Device Drivers for Interrupt-Handling, Memory Device Drivers, On-board Bus Device Drivers, Board I/O Driver.

Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion

(8 Hours)

Module – 5

RTOS and IDE for Embedded System Design: Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques

Summary of the Course: The student will be able to understand the basics of memory, I/O systems and Architecture of an embedded system.

(9 Hours)

Course Outcomes: The students will be able to:

CO1: Understand the basics of memory, I/O systems and Architecture

CO2: Apply the embedded system models, features of processors, memory and I/O systems in developing embedded System.

CO3: Analyze the Real time OS functionality and device drivers used in multitasking embedded applications.

CO4: Design embedded applications using given specifications and concepts of development process

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
A Comprehensive Guide for Engineers and Programmers	Tammy Noergaard	2nd edition,Newnes	2012	Text
Real–Time Systems Design and Analysis	Phillip A. Laplante	Wiley-IEEE Press.	2004	Text
Embedded Systems– A contemporary Design Tool	James K Peckol,	John Weily.	-	Reference

COs and POs Mapping

CO	PO											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1												
CO2		3										
CO3		3										2
CO4			3									2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER - VI

Artificial Neural Networks (3:0:0)3

(Effective from the academic year 2021-22)

Course Code	**21EC644**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the basics of ANN and comparison with biological neuron.
2. Acquire knowledge on Generalization and function approximation of various ANN architectures.
3. Understand reinforcement learning using neural networks.
4. Acquire knowledge of unsupervised learning using neural networks.

Module – 1

Introduction to the course, Significance and scope of ANN, Importance of the course in economic growth of nation. Career perspective in ANN

Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feed forward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks.

(8 Hours)

Module – 2

Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.

Supervised Learning: Perceptron learning and Non-Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search. (8 Hours)

Module – 3

Multi-layered Network Architecture: Back propagation Learning Algorithm, Practical consideration of BP algorithm. Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition. (8 Hours)

Module – 4

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory. (8 Hours)

Module – 5

Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas**.**

Recap/ Summary of all modules

(8 Hours)

Course outcomes:

The students will be able to:

CO1: Understand the role of neural networks in engineering, artificial intelligence, and cognitive modeling.

CO2: Apply the concepts of Neuro-science, Mathematics and Computer Engineering knowledge to perform tasks of neural networks

CO3: Analyse performance of neural network models for given application.

CO4: Design simple neural network models.

Textbook:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
1. Neural Networks A Classroom Approach, , 2nd Edition,	Satish Kumar,	McGraw Hill Education (India) Pvt. Ltd	2009.	**Text**
2. Introduction to Artificial Neural Systems	J.M. Zurada	Jaico Publications	1994.	**Reference**
3. Artificial Neural Networks	B. Yegnanarayana	PHI, New Delhi	1998.	**Reference**

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1												
CO2		2										
CO3			2									
CO4			2									

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Mobile Communication (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC645**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course Objectives:

1. Analyze and design wireless and mobile cellular systems.
2. Understand impairments due to multipath fading channel and be able simulate standard stochastic channel models for various environments.
3. Evaluate the fundamental techniques to overcome the different fading effects.
4. Interpret current and proposed cellular technologies
5. Able to work in advanced research wireless and mobile cellular programs.

Module – 1

SOFTWARE DEFINED RADIO (SDR):

Introduction to SDR: Definitions and potential benefits, software radio architecture evolution – foundations, technology tradeoffs and architecture implications, Antenna for Cognitive Radio.

SDR Architecture: Essential functions of the software radio, architecture goals, quantifying degrees of programmability, top level component topology, computational properties of functional components, interface topologies among plug and play modules, architecture partitions. **(8 Hours)**

Module – 2

INTERFERENCE AND CELL COVERAGE FOR SIGNAL AND TRAFFIC

Introduction to Co-Channel Interference, real time Co-Channel interference, Co-Channel measurement, design of Antenna system, Antenna parameters and their effects, diversity receiver, non-co channel interference different types, Signal reflections in flat and hilly terrain, effect of human made structures, phase difference between direct and reflected paths, constant standard deviation, straight line path loss slope, general formula for mobile propagation over water and flat open area, near and long distance propagation antenna height gain, form of a point to point model**.** **(10 Hours)**

Module – 3

CELL SITE AND MOBILE ANTENNAS

Sum and difference patterns and their synthesis, omni directional antennas, directional antennas for interference reduction, space diversity antennas, umbrella pattern antennas, minimum separation of cell site antennas, high gain antennas, Numbering and grouping, setup access and paging channels channel assignments to cell sites and mobile units, channel sharing and borrowing, sectorization, overlaid cells, non fixed channel assignment, Handoff, dropped calls and cell splitting, types of handoff, handoff invitation, delaying handoff, forced handoff, mobile assigned handoff. Intersystem handoff, cell splitting, micro cells, vehicle locating methods, dropped call rates and their evaluation. **(10 Hours)**

Module – 4

WIRELESS SYSTEMS AND STANDARDS

Second generation, Third generation and Fifth generation Wireless Networks and Standards, WLL, Bluetooth, GSM, IS95, DECT, GSM architecture, GSM channels, multiplex access scheme, TDMA, CDM. **(6 Hours)**

Module – 5

INTELLIGENT NETWORK FOR WIRELESS COMMUNICATIONS

Intelligent cell concept, advanced intelligent network, SS7 network and ISDN for AIN, AIN for mobile communication, asynchronous transfer mode technology, future public land mobile telecommunication system, wireless information superhighway. **(6 Hours)**

Summary of the Course: Course covers the basic concepts of mobile system, Co-channel interference with near end far end interference, Signal reflections in flat and hilly terrain, Effect of

human made structures, concepts of cell coverage for signal and traffic, Cell Site And Mobile Antennas, operation of the various wireless area networks such as GSM,IS-95,GPRS, SMS, and the SS7 network and ISDN for AIN, AIN for mobile communication and application and trends in Mobile Communications.

Course Outcomes: The students will be able to:

CO1: **Apply** the knowledge of mobile system design concepts in wireless mobile communication networks.

CO2: **Analyse** the concepts of Handoff, dropped calls and cell splitting, Intersystem handoff.

CO3: **Design** the Antenna system, Antenna parameters and their effects, diversity receiver, non co-channel Interference different.

CO4: **Interpret** the concepts about Wireless Systems And Standards GSM channels, multiplex access scheme, TDMA, CDMA.

CO5: Perform in a **group** to **design** Intelligent Network For Wireless Communications SS7 network and ISDN for AIN, AIN for mobile communication.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Wireless Communications & 2nd Edition	Theodore .S. Rapport	Pearson Education	2010	Text
Wireless communication	Upen Dalal	oxford University press	2010	Text
Principle of wireless networks	Kaveh Pahlvan, Prashant Krishnamurthy	A United Approach, Pearson Education	2004	Text
"Wireless and Mobile Communications" 3rd Edition	Lee	McGraw Hill	2006	Reference
"Wireless Communications" , 3rd Edition	Theodore. S. Rapport	Pearson Education	2003	Reference

Cos and POs Mapping

COs	POs											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	3											
CO2		3										
CO3			3									
CO4				3					3	3		3
CO5					3				3	3		3

Level3- Highly Mapped,Level 2-ModeratelyMapped, Level1-LowMapped, Level0-NotMapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

VLSI Verification (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC646**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course objectives:

This course will enable students to:

1. Understand the concept of verification and testing and learn the various algorithm.
2. Study the system verification concept.
3. Model different test bench and design the various circuit.
4. Study various coverage used in digital circuit.

Module – 1

Verification techniques:

Introduction to Verification, Testing Vs Verification, Verification Technologies, Functional Verification, Code coverage, Functional coverage. Testbench – Linear Testbench, Linear Random Testbench, Self-checking Testbench, Regression, RTL Formal Verification. (7 Hours)

Module – 2

System Verilog – Data Types & Procedural statements

Introduction to System Verilog, Literal values, data Types, Arrays, Array methods, Creating new types with typedef, user defined structures, enumerated types, attributes, operators, expressions, Procedural statements and control flow, Processes in System Verilog, Task and functions, Routine arguments, Returning from a routine. (7 Hours)

Module – 3

Connecting Testbench and Design

Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment – Generator, Transactor, Driver, Monitor, Checker, Scoreboard

(7 Hours)

Module – 4

Randomization, Assertion and Coverage

Randomization in system Verilog, Constraints, Functional coverage, cross coverage, cover groups, Assertions.

(7 Hours)

Module – 5

Universal Verification Methodology

Introduction to UVM - Verification components - Transaction level modelling UVM – Verification Environments: Developing reusable verification components - Using Verification components – Developing reusable verification environment, developing reusable verification environment – Register classes (12 Hours)

Course Outcomes: The students will be able to:

CO1: Understand the concept of testing and various verification model and learn the basic concept of OOPS.

CO2: Apply the knowledge of testbench and design the digital circuit.

CO3: Analyse different algorithms used for verification.

CO4: Interpret the given case study situation related to applications of real time life.

CO5: Perform in a **group** to make effective **presentation** on the topics related to applications of digital circuit.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Getting started with UVM: A Beginner's Guide, First Edition	Vanessa R. Copper	Verilab Publishing.	2013	Text
System Verilog for Verification: A guide to learning the Testbench language features, Third Edition	Christian B Spear	, Springer publications.	2012	Text
Writing Testbenches using System Verilog, First Edition	Janick Bergeron	Springer Publications	2006	Reference
The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, First Edition	Ray Salmei	Boston Light Press	2013	Reference

COs and POs Mapping

COs	PO's											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	2											
CO2	3											
CO3		3										
CO4									2	2		
CO5									2	2		2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

CHOICE BASED CREDIT SYSTEM (CBCS)

SEMESTER - VI

Cellular Mobile Communication (3:0:0) 3

(EFFECTIVE FROM THE ACADEMIC YEAR 2021-22)

Course Code	**21EC651**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the application of multi user access in a cellular communication scenario.
2. Understand the propagation mechanisms in an urban mobile communication using statistical and empirical models.
3. Understand system architecture, call processing protocols and services of GSM, GPRS and EDGE.
4. Understand system architecture, call processing protocols and services of CDMA

Module – 1

Introduction: Significance and scope, Importance in the economic growth of the nation. Career perspectives. Impact on national economy, state of art and future directions in mobile communication.

Cellular Concept: Frequency Reuse, Channel Assignment Strategies, Interference and System Capacity, Power Control for Reducing Interference, Trunking and Grade of Service, Improving Capacity in Cellular Systems. Mobile Radio Propagation: Large Scale path Loss- Free Space Model, Three basic propagation mechanisms, Practical Link Budget Design using Path Loss Models.

Self-Study: Outdoor Propagation Models

(8 Hours)

Module – 2

Mobile Radio Propagation: Small-Scale Fading and Multipath: Small scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Rician Distributions, Statistical Model for Multipath Fading Channels (Clarke‘s Model for Flat Fading only).

(8 Hours)

Module – 3

System Architecture and Addressing: System architecture, The SIM concept, Addressing, Registers and subscriber data, Location registers (HLR and VLR) Security-related registers (AUC and EIR), Subscriber data, Network interfaces and configurations. Air Interface – GSM Physical Layer: Logical channels, Physical channels, Synchronization- Frequency and clock synchronization, Adaptive frame synchronization, Mapping of logical onto physical channels, Radio subsystem link control, Channel coding, source coding and speech processing, Source coding and speech processing, Channel coding, Power-up scenario. GSM Protocols: Protocol architecture planes, Protocol architecture of the user plane, Protocol architecture of the signalling plane, Signalling at the air interface (Um), Signalling at the A and Abis interfaces, Security-related network functions, Signalling at the user interface.

(8 Hours)

Module – 4

GSM Roaming Scenarios and Handover: Mobile application part interfaces, Location registration and location update, Connection establishment and termination, Handover.

Services: Classical GSM services, Popular GSM services: SMS and MMS. Improved data services in GSM: GPRS, HSCSD and EDGE GPRS System architecture of GPRS , Services , Session management, mobility management and routing, Protocol architecture, Signalling plane, Interworking with IP networks, Air interface, Authentication and ciphering, Summary of GPRS . HSCSD: Architecture, Air interface, HSCSD resource allocation and capacity issues. EDGE: The EDGE concept, EDGE physical layer, modulation and coding, EDGE: effects on the GSM system architecture, ECSD and EGPRS.

(8 Hours)

Module – 5

CDMA Technology: Introduction to CDMA, CDMA frequency bands, CDMA Network and System Architecture, CDMA Channel concept, Forward Logical Channels, Reverse logical Channels, CDMA frame format, CDMA System Operations (Initialization/Registration), Call Establishment, CDMA Call handoff, IS95B, CDMA2000, W-CDMA, UMTS, CDMA data networks, Evolution of CDMA to 3G,

Self-study: CDMA 2000 RAN Components, CDMA 2000 Packet Data Service.

Recap/Summary of all the modules.

(8 Hours)

Course outcomes: The students will be able to:

CO1: Apply the understanding of statistical characterization of urban mobile channels to compute the performance for simple modulation schemes.

CO2: Describe the limitations of GSM, GPRS and CDMA to meet high data rate requirements and limited improvements that are needed.

CO3: Analyze the call process procedure between a calling number and called number for all scenarios in GSM or CDMA based systems

CO4: Present in a team, the recent developments in Cellular communication technology

Textbooks:

1. Theodore Rapport, "Wireless Communications – Principles and Practice", Prentice Hall of India, 2nd Edition, 2007.
2. Jorg berspacher, Hans-Jorg Vogel, Christian Bettstetter, Christian Hartmann, "GSM– Architecture, Protocols and Services", Wiley, 3rd Edition, 2009.
3. Gary J Mullet, "Introduction to Wireless Telecommunications Systems and Networks" , Cengage Learning.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Wireless Communications – Principles and Practice, 2nd Edition	Theodore Rapport	Prentice Hall of India	**2007**	**Text**
GSM– Architecture, Protocols and Services, 3rd Edition	Jorg berspacher, Hans-Jorg Vogel, Christian Bettstetter, Christian Hartmann,	Wiley	**2009**	**Text**
Introduction to Wireless Telecommunications Systems and Networks,1st edition	Gary J Mullet	Cengage Learning	2006	**Reference**

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1		2										
CO2												
CO3			2									
CO4										1	1	1

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER -VI

Sensors and Applications (3:0:0) 3
(Effective from the academic year 2021-22)

Course Code	**21EC652**	CIE Marks	50
Teaching Hours/Week (L:T:P):	3:0:0	SEE Marks	50
Total Number of Lecture Hours	40	Exam Hours	03

Course objectives:

1. Understand the working of different types of transducers and sensors.
2. Describe recent trends in sensor technology and their selection.
3. Undertake complex and unstructured problem-solving real time challenges using sensors.
4. Have a multidisciplinary experience, integrating knowledge of courses in Electronics and Telecommunication engineering.

Module – 1

Introduction: Introduction to sensors and Applications; its significance and scope in the current scenario. Industrial applications, research and innovations related to sensors. Impact of the course on society problems, sustainable solutions, and national economy.

Sensors and Transducers:
Introduction, Classification of Transducers, Advantages and Disadvantages of Electrical Transducers, Transducers Actuating Mechanisms, Resistance Transducers, Variable Inductance Transducers, Capacitive Transducers, Piezoelectric Transducers, Hall Effect Transducers, Thermoelectric Transducers, Photoelectric Transducers.

(8 Hours)

Module – 2

Sensors and Transducers (continued):
Stain Gages, Load Cells, Proximity Sensors, Pneumatic Sensors, Light Sensors, Tactile Sensors, Fiber Optic Transducers, Digital Transducers, Recent Trends – Smart Pressure Transmitters, Selection of Sensors, Rotary – Variable Differential Transformer, Synchros and Resolvers, Induction Potentiometers, Micro Electromechanical Systems.

(8 Hours)

Module – 3

Data Acquisition Systems and Conversion:
Introduction, Objectives and Configuration of Data Acquisition System, Data Acquisition Systems, Data Conversion.
Data Transmission and Telemetry: Data/Signal Transmission, Telemetry. Measurement of Non – Electrical Quantities: Pressure Measurement

(8 Hours)

Module – 4

MCUs and DSPs for sensor:
Introduction, MCU control, MCUs for sensor interface, DSP control, Software, tools and support, sensor integration.

(8 Hours)

Module – 5

Sensor Communication and MEMS:
Wireless zone sensing, surface acoustical wave devices, intelligent transportation system, RF-ID, Micro optics, micro-grippers, micro-probes, micro- mirrors, FEDs, communications for smart sensors - sources and standards, automotive protocols, industrial networks, office and building automation, home automation, protocols in silicon, other aspects of network communications.
Summary of the Course: students will be acquire knowledge in different types of sensors and sensor communications along with MEMS.

(8 Hours)

Course outcomes: The students will be able to:

CO1: Understand the understanding of working of various transducers and sensors, recent technologies.

CO2: Apply the knowledge gained in the developing different sensor applications.
CO3: Analyze the use of smart sensors in communication, MEMS and automation.
CO4: Interpret the given case study situation related to applications of sensors.
CO5: Perform in a **group** to **build** a small application and prepare the report for the same.

Textbooks / References

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Electrical and Electronic Measurements and instrumentation, 3rd Edition	R.K Rajput	S. Chand Publications	2013	Text
Understanding Smart Sensors, 2nd Edition	Randy Frank	Artech House Publications	2013	Text
Micro and Smart Systems: Technology and modelling	G. K. Ananthasuresh et.al.	Wiley Publications	2012	Reference
A Course in Electronics and Electrical Measurements and Instruments, 13th Edition	J.B. Gupta	Katson Books Publications	2008	Reference

CO and PO Mapping

COs	POs											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	3											
CO2			3	2								
CO3		3		2								
CO4		2		2								
CO5					2				3	3		3

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

Signal Processing and Applications (3:0:0) 3
(Common to ECE, ETE & EEE Branches)
(Effective from the academic year 2021-22)

Course Code	**21EC653**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course Objectives:
This course will enable students to:

1. Understand the fundamentals of signal processing.
2. Familiar with DSP techniques in frequency domain.
3. Use toolbox in the MATLAB software to write programs to perform various applications of signal processing.

Module – 1

Introduction: Introduction to Signal processing, significance and scope of signal processing in current scenario, industry applications, research and innovations related to signal processing, impact on course on societal problems**.**

Classification of signals: Classification of signals and operations of signals.

System Classification and properties: Linear-nonlinear, Time variant-invariant, causal-non causal, static-dynamic, stable- unstable, invertible

(9 Hours)

Module – 2

Analysis of LTI system in various domains: Convolution sum & Integral definition with basic problems, Z transform definition with basic problems, Introduction to Fourier Transform & DTFT, Definition and basic problems. Sampling Theorem- Statement and

proof, converting the analog signal to a digital signal. Practical sampling. Applications

(7 Hours)

Module – 3

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, properties (no proof) and basic problems
Fast-Fourier-Transform (FFT) algorithms: Radix-2 FFT algorithms for the computation of DFT decimation-in-time algorithms.
Application (7 Hours)

Module – 4

Digital Filter Design:
Frequency response of ideal analog filters, Salient features of Butterworth filters, Design and implementation of Analog Butterworth filters to meet given specifications.

Design of FIR Filters using the Window technique: rectangular, hamming and the frequency sampling technique to meet given specifications. Applications

(8 Hours)

Module – 5

Applications of signal processing:
Introduction to image, bio medical signals. Case study on image, bio medical signal processing applications using MATLAB.
Summary of the Course: This course provides basic signal processing techniques in various domains and applications using MATLAB. (9 Hours**)**

Course Outcomes: The students will be able to:
CO1: Apply the knowledge of digital signal processing to find DFT's of various signals .
CO2: Design various digital filters.

CO3: Interpret the given case study material related to different operations and properties of signals and systems in various domains.
CO4: Demonstrate in team simple projects of Signal processing applications with ideas

Textbooks/Reference:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Signals and System 2nd Edition	Simon Haykins and Barry Van Veen	Wiley India	2008	**Text**
Proakis & Monalakis, 4th Edition	Digital signal processing Principles Algorithms & Applications	Pearson education, New Delhi	2007	**Text**
Digital Image Processing	Ayaraman, S.Esakkirajan, T.Veerakumar,	Tata Mc GrawHill		**Reference**
Biomedical Signal and Image Processing, Second edition	Kayvan Najarian , Robert Splinter	CRC Press, Taylor & Francis Group, LLC	2012	**Reference**

COs and POs Mapping

COs	PO's											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1												
CO2		2										
CO3			3									
CO4					3					2		2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING
Choice Based Credit System (CBCS)
SEMESTER - VI

Embedded Controllers and Applications (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC654**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Lecture Hours	40	Exam Hours	03

Course Objectives:

This course will enable students to:

Understand, differentiate, classify, and identify different purposes of embedded systems in which they evolved.

Analyze the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.

Discuss the hardware /software co-design approaches.

Demonstrate the applications of embedded controller systems as related to the industry trends.

Module – 1

Introduction: Introduction to embedded systems, significance and scope of embedded system in current scenario, industry applications, research and innovations related to embedded system, impact of course on societal problems.

Introduction to embedded controllers:

Introduction to embedded controller systems starting from definition of embedded system, embedded system vs general computing systems, history, classification, major application areas, and wearable devices-the innovative bonding of lifestyle with embedded technologies.

(8 Hours)

Module – 2

Typical embedded system:

Elements of embedded system, Analog and digital electronic components-Logic gates, Mux,De-Mux, Encoder, Decoder, Buffer ,Latch. Core of the embedded system, Sensors, Actuators, I/O Subsystem-Led,7-segment LED display, Optocoupler, Stepper motor, Relay, Piezo Buzzer, Push Button Switch, Keyboard. Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only), embedded firmware.

(8 Hours)

Module – 3

Embedded Systems-Application- and Domain Specific:

Application specific (Washing machine), Automotive domain examples, factors to be considered in selecting a controller.

Hardware Software Co-Design and Program Modelling: Fundamental issues in hardware software co-design, computational models in embedded design (excluding UML), hardware software trade-offs. (8 Hours)

Module – 4

Embedded Product Development Life cycle (EDLC):

What and Why is EDLC, Objectives, Different Phases, EDLC approaches (Modelling the EDLC)

(8 Hours)

Module – 5

Industry Trends:

Processor trends in embedded system, Embedded OS trends, Development language trends-beyond embedded C, Open standards, Frameworks and Alliances, Bottlenecks, Development Platform Trends, Cloud, Internet of Things (IoT) and Embedded Systems-The Next Big Thing

Summary of the Course: Course covers the basic concepts on embedded controller systems, applications and the trends in the embedded industry.

(8 Hours)

Course outcomes: The students will be able to:

CO1: Understand the basic concepts of embedded controller systems.
CO2: Apply the knowledge of embedded controller systems and be able to differentiate, classify and identify various embedded systems.
CO3: Analyse the role of sensors, actuators, and their interfacing with I/O subsystems of embedded system.
CO4: Discuss the different computational models used in embedded system design.
CO5: Interpret the given case study material related to the product development of embedded controller systems in various domains
CO6: Perform an activity as related to industrial applications of embedded controller systems.

Textbooks*:*
1. K V Shibu, "Introduction to Embedded Systems" 2nd Edition , McGraw Hill, 2016.

References:
1. Yifeng Zhu," Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Edition, Man Press LLC ,2015.
2. Rajkamal, "Embedded Systems" 2nd Edition, McGraw Hill Publications, 2010.

COs and POs Mapping

COs	PO's											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1												
CO2		3										
CO3			3									
CO4	2											
CO5				2								
CO6										2		2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING
Choice Based Credit System (CBCS)
SEMESTER – VI

8051 Microcontroller (3:0:0) 3
(Effective from the academic year 2021-22)

Course Code	**21EC655**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course Objectives:

This course will enable students to:

1. Understand the difference between Microprocessor and Microcontroller
2. Learn instruction sets to write various assembly programs
3. Comprehend the operation and use of inbuilt Timers/Counters and Serial port of 8051
4. Interface 8051 to external memory and I/O devices using its I/O ports

Module – 1

8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.

(8 Hours)

Module – 2

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. **(8 Hours)**

Module – 3

8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops - Delay subroutine, Factorial of an 8 bit number (result maximum 8 bit), Block move without overlap, Addition of N 8 bit numbers, Picking smallest/largest of N 8 bit numbers.

Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status**. (8 Hours)**

Module – 4

8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially. **(8 Hours)**

Module – 5

8051 Interrupts and Interfacing Applications: 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, LCD and Stepper motor and their 8051 Assembly language interfacing programming.

Summery/Recap of all the modules

(8 Hours)

Course Outcomes: The students will be able to:

CO1: Understand and differentiate the Architecture of microprocessor and microcontroller.

CO2: Analyze and Apply instructions for assembly programs.

CO3: Analyze the functions of on-chip peripherals.

CO4: Develop a small embedded system.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
8051 Micro controller and Embedded System	Muhammad Ali Mazidi and Janice Gillispi Mazidi	Pearson Education Publication	2nd Edition, 2006	Text
Advanced Microprocessors and Peripherals	A.K. Ray and K.M. Bhurchandi	TMH, 3rd Edition	2012	Text
The 8051 Microcontroller Based Embedded Systems	Manish K Patel	McGraw Hill, 1st Edition	2014	Reference
Microcontrollers: Architecture, Programming, Interfacing and System Design	Raj Kamal	Pearson Education	3rd Edition, 2005	Reference

COs and POs Mapping

COs	PO's											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1	1											
CO2		3										
CO3		3										
CO4			3							1		1

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Industrial Electronics (3:0:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC656**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course Objectives:

This course will enable students to:

1. Understand the basics of the working of thyristors, regulated power supply, Programmable logic arrays, heating and welding control.
2. Study the applications of power semiconductor devices to control the power.
3. Learn the simulation of power electronics circuits.

Module – 1

Introduction: Scope of the industrial electronics, Importance of the power electronics in the economic growth of nation and sustainable solutions related to the industrial electronics. Current trends in industrial electronics.

Power Semiconductor Devices: Introduction, Control Characteristics of Power Devices, types of Power Electronic Circuits.

Thyristors: Introduction, Principle of Operation of SCR, Static Anode-Cathode Characteristics of SCR, two transistor model of SCR, Gate Characteristics of SCR, Turn-On Methods, Turn-Off Mechanism, Turn-Off Methods: Natural and Forced Commutation

(8 Hours)

Module – 2

Regulated Power Supplies: Performance parameters of power supply, Zener diode voltage regulator, Transistorised series voltage regulator, op-amp voltage regulators, Transistorised shunt voltage regulator, The 723/723C Voltage regulator, Three terminal IC voltage regulators.

(8 Hours)

Module – 3

Motor Control: Introduction, AC Voltage Controllers**-** Principles of ON-OFF Control, Principle of Phase Control, Single phase control, Phase control of DC motor. AC power control of a Lamp dimmer.

(8 Hours)

Module – 4

Heating and Welding Control: Introduction, Induction Heating-Theory and principle, of induction heating, Effects of supply Frequency and source voltage on induction heating, Choice of frequency for induction Heating.

Welding – Theory of Resistance welding, classification of resistance welding, Scheme for AC Resistance welding. (8 Hours)

Module – 5

Programmable Logic Controller: Introduction, functions and applications of PLC, Comparison of data processing computer with the process control computer system. Functional Block diagram of PLC, Microprocessor of a programmable Logic controller.

Recap/Summary of the Course. (8 Hours)

Course Outcomes: The students will be able to:

CO1: Apply the knowledge of Programmable Logic Controller, heating and welding in controlling applications.

CO2: Analyse power semiconductor-based Circuits to control the AC and DC power

CO3: Interpret the given case study material related to the application of industrial electronics

CO4: Simulate power semiconductor-based circuits using CAD.

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
Industrial Electronics and control & 3rd Edition	Biswantha Paul	PHI Learning Private Limited	2014	Text
Power Electronics, Circuits, Devices and Applications", Pearson Education & 4th Edition	Mohammad H Rashid	- Pearson Education	2014	Reference
Electronic Devices and circuits & 6th Edition	Theodore. H. Bogart	Pearson Education	2004	Reference

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	3											
CO2		2										
CO3			3									
CO4										3		2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Advanced Communication Theory (2:2:0) 3

(Effective from the academic year 2021-22)

Course Code	**21EC67**	CIE Marks	50
Teaching Hours/Week (L:T:P)	2:2:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	03

Course objectives:

This course will enable the Students to:

1. Learn the characteristics of RF communication and Digital modulation.
2. Understand the basics of antennas and signalling over the channels.
3. Know the parameters required for antenna radiation and digital communication.
4. Acquire the knowledge of different antennas and digital modulation techniques.

Introduction: Importance of RF communication, digital communication, Significance and Scope of the course in economic growth of Nation, Impact of the course on Societal Problems, Career Perspective, Innovations, Research status/trends.

Module – 1

Antenna Basics:

Basic antenna parameters, patterns, beam area, Radiation intensity, Beam efficiency, directivity and gain, Radio communication link, Polarization.

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Field Patterns, Phase Patterns, Arrays of Two Isotropic Point Sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.

(8 Hours)

Module – 2

Electric dipole:

Fields of short dipole, Radiation resistance of short dipole, Thin linear antenna and Radiation resistance of $\lambda/2$ dipoles.

Types of Antennas:

Horn antenna, Parabolic antenna, Helical antenna, Yagi-Uda array, Log-periodic antennas.

(8 Hours)

Module – 3

Micro-strip antennas:

Basic characteristics, Feeding Methods, Rectangular patch, circular patch, Q- factor, Bandwidth and efficiency, coupling, circular polarization.

Self Study: Simulation of microstrip antennas for wireless communication.

Band-pass Signal to Equivalent Low-pass:

Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of band-pass signals, Complex low pass representation of band-pass systems, Complex representation of band pass signals and systems.

(8 Hours)

Module – 4

Signalling over AWGN Channels:

Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.

(8 Hours)

Module – 5

Digital Modulation Techniques:

Phase shift Keying techniques using coherent detection: generation, detection and error

probabilities of BPSK and QPSK, M-ary PSK, M-ary QAM.

Frequency shift keying techniques using coherent detection: BFSK, DPSK symbol representation, Block diagram treatment of Transmitter and Receiver, probability of error(without derivation of probability of error equation)

Summary of the Course: The student will be able to explore the concepts of RF communication and digital communication.

(8 Hours)

Course outcomes: The students will be able to:

CO1**: Understand** the basic characteristics of antenna theory and digital communication

CO2: Apply various properties/laws /knowledge of microwave and digital communication to solve the problems related to communication system

CO3: Analyse the behaviour of antenna and modulation technique parameters required for wireless propagation

CO4: Design different antennas and digital modulation schemes

CO5: Interpret the given case study situation related to the wireless communication

CO6: Perform in a **group** to **design** different digital modulation techniques and microstrip antennas using **MATLAB**/**Simulink** and **HFSS tool.**

Textbooks*:*

1. John D. Kraus, "Antennas for all practical applications",4th Edition, McGraw Hill, 2011.
2. Simon Haykin**,** "Digital Communication Systems"**,** 1Edition, John Wiley & sons, 2014.

References :

1. Stutzman & Thiele , **"**Antenna Theory & Design" 2nd Edition**,** Wiley, 2010.
2. B.P.Lathi and Zhi Ding **, "**Modern Digital and Analog communication Systems"**,** 4th Edition, Oxford University Press, 2010.
3. Simon Haykin, "Digital Communication", John Wiley India Pvt. Ltd, 2009.

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	1											
CO2	2											
CO3		2										
CO4			3									
CO5				3					2	3		3
CO6					2				3	3		3

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

VLSI Design (4:0:0) 4

(Effective from the academic year 2021-22)

Course Code	**21EC68**	CIE Marks	50
Teaching Hours/Week (L:T:P)	4:0:0	SEE Marks	50
Total Number of Contact Hours	50	Exam Hours	03

Course Objectives: This course will enable students to:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Learn the operation principles and analysis of inverter circuits.
3. Design Combinational, sequential and dynamic logic circuits as per the requirements
4. Infer the operation of Semiconductors Memory circuits.
5. Demonstrate the concepts of CMOS testing

Module – 1

Introduction: A Brief History and scope of VLSI, impact of semiconductor industry on societal problem and economy, career perspective in VLSI domain, trends in VLSI, MOS Transistors, CMOS Logic

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics. (10 Hours)

Module – 2

Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction of CMOS Technologies, Layout Design Rules, layout examples.

Self-Study: MOSFET scaling (10 Hours)

Module – 3

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths

Combinational Circuit Design: Introduction, Circuit families. (10 Hours)

Module – 4

Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques.

(10 Hours)

Module – 5

Semiconductor Memories: Introduction, Dynamic Random-Access Memory (DRAM) and Static Random-Access Memory (SRAM).

Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability,

Recap: MOS transistor theory, fabrication, combinational and sequential circuit design, dynamic circuits, MOS transistor theory, fabrication, combinational and sequential circuit design.

Self-Study: VLSI companies and job profiles in India and abroad

(10 Hours)

Course Outcomes: The students will be able to:

CO1: Understand MOS transistor theory, CMOS fabrication flow and technology scaling, stick and layouts concepts.

CO2: Apply the knowledge of combinational, sequential logic circuits, and layouts to design digital circuits.

CO3: Analyse testing, testability issues and memory elements along with timing considerations in VLSI Design

CO4: Interpret the given case study material related to design and demonstrate an of Digital sub system.

CO5: Design vlsi digital system and make effective presentation in a group**.**

Text Books/References:

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
CMOS Digital Integrated Circuits: Analysis and Design	Sung Mo Kang & Yosuf Leblebici	Tata McGraw-Hill	2002	Text
CMOS VLSI Design- A Circuits and Systems Perspective	Neil H. E. Weste, and David Money Harris	Pearson Education, 4th edition	2011	Text
Microelectronics Circuits Theory and Applications	Adel Sedra and K. C. Smith	Oxford University Pres, , 6th or 7th Edition	2009	Reference
Basic VLSI Design	Douglas A Pucknell & Kamran Eshragian	PHI, 3rd Edition	1994	Reference

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	3											
CO2		3										
CO3			3									
CO4				2								
CO5									3		3	3

Level 3- Highly Mapped, Level 2-Modertely Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER – VI

Advanced Communication Laboratory (0:0:2) 1

(Effective from the academic year 2021-22)			
Course Code	**21ECL69A**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:0:2	SEE Marks	50
Total Number of Contact Hours	26	Exam Hours	03

Course objectives:

This course will enable students to

1. Understand the circuits for the generation of digital Modulation and demodulation schemes viz; FSK, PSK, QPSK, DPSK.
2. Use modern tools to evaluate the performance of digital modulation techniques.

Experiments using Hardware

1. Generation and detection of BPSK, FSK
2. Generation and detection of QPSK, DPSK
3. Generation and detection of different Line codes.
4. Conduct an experiment to measure transmission loss, bending loss, NA of an optical fiber communication system**.**
5. Determination of the VSWR and Power loss of circulator and isolator
6. Measurement of VSWR and Power loss of directional coupler and E, Hplane tees
7. Measurement of impedance using slotted line assembly

Field intensity measurement of a Horn antenna

Experiments using Software (MAT LAB, SCI LAB, LAB VIEW etc)

1. Conduct an experiment to evaluate the performance (BER) of BPSK, FSK.

Conduct an experiment to evaluate the performance (BER) of QPSK, M-ary QAM

Open Ended Experiments

1. Demonstrate the application of different digital modulation techniques in various wireless communication systems, like GSM, LTE, WLAN, Wi – fi etc.
2. Field intensity measurement of a Parabolic antenna
3. Determination of the VSWR and Power loss of Magic tee
4. Prove Reciprocity Theorem of an Antenna
5. Determination of type of antenna as good Transmitter or Receiver

Course outcomes: The students will be able to

CO1:	**Conduct** experiments to measure different parameters related to microwave devices, components and antennas using microwave bench at RF range.
CO2:	**Apply** the knowledge of electronic circuits for the generation and detection of various modulation schemes.
CO3:	**Analyze** the performance of digital modulation techniques in the presence of noise at the receiver.
CO4:	**Write a report** for the conducted experiment.
CO5:	**Conduct** open ended experiments to measure/check the characteristics of RF devices/components

COs and POs Mapping

COs	POs											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	2											
CO2	3											
CO3		3										
CO4										2		
CO5												2

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

Choice Based Credit System (CBCS)

SEMESTER - VI

VLSI Laboratory (0:0:2) 1

(Effective from the academic year 2021-22)

Course Code	**21ECL69B**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:0:2	SEE Marks	50
Total Number of Contact Hours	26	Exam Hours	3

Course Objectives: This course will enable students to:

1. Design, model, simulate and verify CMOS digital circuits
2. Design layouts and perform physical verification of CMOS digital circuits
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
4. Perform RTL-GDSII flow and understand the stages in ASIC design

Part – A
Analog Design

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:
   I. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?
   II. From the simulation results compute tpHL, tpLH and td for all three Geometrical settings of width?
   III. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?
1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a)Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B
Digital Design

1. Write Verilog code for 4-bit up/down asynchronous reset counter and carry out the following:

a. Verify the functionality using test bench

b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write Verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical

path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.

3. Write Verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioural modelling.

a. Perform functional verification using test bench

b. Synthesize the design targeting suitable library by setting area and timing constraints.

c. For various constrains set, tabulate the area, power and delay for the synthesized netlist.

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints. Compare the synthesis results of ALU modelled using IF and CASE statements

4. Write Verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

5. For the synthesized netlist carry out the following for any two above experiments:

a) Floor planning (automatic), identify the placement of pads
b) Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
c) Physical verification and record the LVS and DRC reports
d) Perform Back annotation and verify the functionality of the design
e) Generate GDSII and record the number of masks and its color composition.

Course outcomes: The students will be able to:

CO1: Design the analog circuits with minimum delay by changing the width of NMOS and PMOS width (Wn and Wp) using EDA tool.

CO2: Design the circuit using optimum layout method and compare the circuit performance with post layout simulation.

CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list.

CO4: Perform an experiment individually and comprehend, write and reproduce the results.

Question paper pattern:

- The question paper will have two experiments to be conducted.
- Each full question will be for 50 marks.

Conduction of the experiments carries 70% of the total marks. Writeup and Viva carries 15% each of the total marks.

Title & Edition	Author	Publisher	Year of Publication	Text / Reference
CMOS Digital Integrated Circuits: Analysis and Design	Sung Mo Kang & Yosuf Leblebici	Tata McGraw-Hill	2002	Text
CMOS VLSI Design- A Circuits and Systems Perspective	Neil H. E. Weste, and David Money Harris	Pearson Education, 4th edition	2011	Text

COs and POs Mapping

COs	POs											
	1	2	3	4	5	6	7	8	9	10	11	12
CO1			3									
CO2				3								
CO3					3							
CO4								3	3		3	3

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped